

174/205

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Martin Langhammer  
Application No. : 09/826,527 Confirmation No. : 2831  
Filed : April 4, 2001  
For : DSP PROCESSOR ARCHITECTURE WITH WRITE  
DATAPATH WORD CONDITIONING AND ANALYSIS  
Group Art Unit : 2121

New York, New York  
January 9, 2002

Hon. Commissioner for Patents  
Washington, D.C. 20231

TRANSMITTAL LETTER FOR SUPPLEMENTAL  
INFORMATION DISCLOSURE STATEMENT

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Sir:

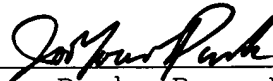
Transmitted herewith is a Supplemental  
Information Disclosure Statement to be filed in the  
above-identified patent application. This Statement is  
being submitted:

- ☐ within three months of the application filing date;
- ☒ more than three months from the application filing date but before the mailing date of the first Office Action on the merits.

In accordance with 37 C.F.R. § 1.97, submission  
of this Statement requires no fee. However, if for any  
reason a fee is due, the Director of the United States

Patent and Trademark Office is hereby authorized to charge payment of any fees required in connection with this Supplemental Information Disclosure Statement to Deposit Account No. 06-1075. A duplicate copy of this transmittal letter is transmitted herewith.

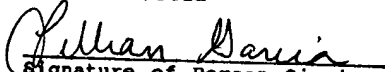
Respectfully submitted,

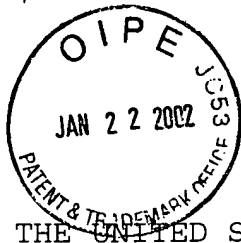


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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. §§ 1.56 and 1.97  
applicant wishes to call the attention of the Examiner to  
the following references:

U.S. Patents

|              |          |                  |
|--------------|----------|------------------|
| 3,473,160    | 10/14/69 | Wahlstrom        |
| 4,871,930    | 10/03/89 | Wong et al.      |
| 4,912,345    | 03/27/90 | Steele et al.    |
| 5,122,685    | 06/16/92 | Chan et al.      |
| 5,128,559    | 07/07/92 | Steele           |
| 5,371,422    | 12/06/94 | Patel et al.     |
| 5,483,178    | 01/09/96 | Costello et al.  |
| 5,689,195    | 11/18/97 | Cliff et al.     |
| 5,754,459    | 05/19/98 | Telikepalli      |
| 5,825,202    | 10/20/98 | Tavana et al.    |
| 5,874,834    | 02/23/99 | New              |
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| 09/124,649 | 07/29/98 | Ngai et al.       |
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| 09/955,645 | 09/18/01 | Langhammer et al. |
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### Foreign Patent Documents

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| 0 461 798 A2 | 12/18/91 | EPO |
| 2 283 602 A  | 05/10/95 | GB  |

### Other Documents

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"Xilinx Unveils New FPGA Architecture to Enable  
High-Performance, 10 Million System Gate Designs",  
Xilinx Virtex-II Architecture Technology  
Background, Xilinx Inc., June 22, 2000, pp.1-9.

"Xilinx Announces DSP Algorithms, Tools and Features  
for Virtex-II Architecture", Xilinx Inc., November  
21, 2000, pp. 1-4.

"Virtex-II 1.5V Field-Programmable Gate Arrays",  
Advance Product Specification, DS031-2 (v1.3),  
Xilinx Inc., January 25, 2001, Module 2 of 4,  
pp. 1-50.

"Virtex-II 1.5V Field-Programmable Gate Arrays",  
Advance Product Specification, DS031-1 (v1.5),  
Xilinx Inc., April 2, 2001, Module 1 of 4, pp. 1-7.

"Virtex-II 1.5V Field-Programmable Gate Arrays",  
Advance Product Specification, DS031-2 (v1.5),  
Xilinx Inc., April 2, 2001, Module 2 of 4, pp. 1-36.

These references are also listed on the attached Form  
PTO-1449 (submitted in duplicate), and copies of them are  
enclosed.

Consideration of the foregoing in relation to  
this patent application is respectfully requested.

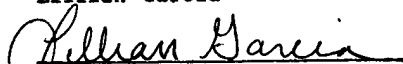
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